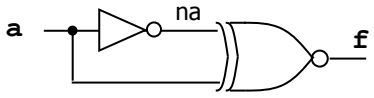
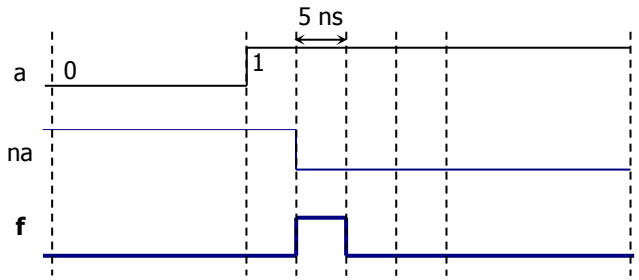
Solutions - Quiz 1

(January 24th @ 5:30 pm)

Problem 1 (30 pts)

- Complete the timing diagram of the digital circuit shown below. You must consider the propagation delays. Assume the propagation delay of every gate is 5 ns. The initial values of all signals are plotted in the figure.





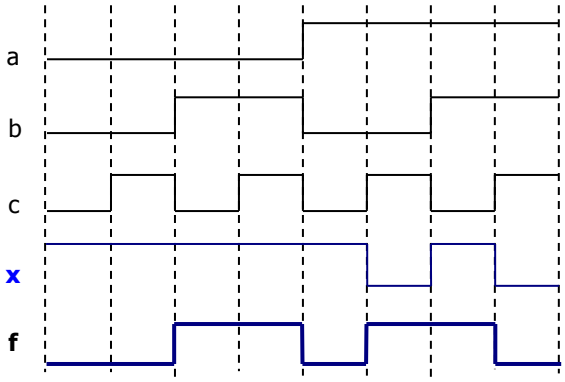
Problem 2 (30 pts)

- Complete the timing diagram of the logic circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;

entity test is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end test;

architecture struct of test is
  signal x: std_logic;
begin
  f <= x xnor b;
  x <= a nand c;
end struct;
```



Problem 3 (40 pts)

- Design a 3-input circuit that generates a '0' when two or more of the inputs are '0'. It also generates a '1' when two or more of the inputs are '1'. Complete the truth table, provide the simplified Boolean expression of the circuit, and sketch the minimized circuit.

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

z \ xy	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$f = xy + yz + xz$